WEST Search History

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DATE: Wednesday, August 25, 2004

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	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
☐	L22	l1.ab. and L18	2
☐	L21	l1.clm. and L18	0
☐	L20	l1 and L18	21
☐	L19	l2 and L18	2
☐	L18	l12 or l13 or l14 or l15 or l16 or l17	4258
☐	L17	708/801.ccls.	409
☐	L16	708/800.ccls.	150
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☐	L14	713/1.ccls.	1386
☐	L13	713/100.ccls.	790
☐	L12	710/100.ccls.	1139
☐	L11	function$7 same ((coupl$4 or decoupl$4) near2 (analog adj blocks))	3
☐	L10	(analog adj function) same ((coupl$4 or decoupl$4) near2 (analog adj blocks))	3
☐	L9	(analog adj function) same ((combine or combining or combination) near2 (analog adj blocks))	1
	DB=USPT; PLUR=YES; OP=OR		
☐	L8	6507214.pn.	1
☐	L7	US-6765407-B1.did.	1
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☐	L6	l2 and L5	6
☐	L5	(selectiv$4 or electrical$4) near3(coupl$7 or decoupl$7)	132833

☐	L4	((selectiv$4 or electrical$4) near3(coupl$7 or decoupl$7) near5 (analog adj blocks))	4
☐	L3	L2 same ((single or one) near2 (ic or (integrated adj circuit)))	2
☐	L2	((plurality or multiple) near2 analog near2 blocks)	59
☐	L1	((multi-function) adj (device or peripheral))	670

END OF SEARCH HISTORY

Goreeki

DOCUMENT-IDENTIFIER: US 5574678 A
TITLE: Continuous time programmable analog block architecture

Brief Summary Text (9):
By removing the sensitivity to an interconnection array and facilitating internal modification of function without changing the topologic sensitivity to offset and distortion, an integrated circuit can advantageously be provided with multiple programmable analog circuit blocks and an interconnection array which can accommodate more complex analog functions.

Drawing Description Text (3):
FIG. 2 shows a schematic block diagram of the interconnection of a plurality of programmable analog circuit blocks to provide a programmable analog circuit in accordance with the present invention.

Detailed Description Text (3):
Referring to FIG. 1, programmable analog circuit system 20 includes a plurality of programmable analog circuit blocks (i.e., PACell circuits) 22, as well as interconnection array 24, memory 26 and reference voltage circuit 28. Each programmable analog circuit block 22 is coupled to interconnection array 24. Additionally, memory 26 and reference voltage circuit 28 are coupled to interconnection array 24.

Detailed Description Text (9):
Referring to FIG. 2, a more detailed view of programmable interconnection array 24 is shown. Programmable interconnection array 24 includes a plurality of connection points 40. Because of the input and output properties of the programmable analog circuit block, specifically, high input impedance and low output impedance, multip

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L3: Entry 1 of 2 File: USPT Mar 2, 2004

Gorecki et al

DOCUMENT-IDENTIFIER: US 6701340 B1
TITLE: Double differential comparator and programmable analog block architecture using same

Brief Summary Text (7):
Programmable analog integrated circuits such as those disclosed in the Gorecki patent, typically include analog circuit blocks interconnected by a programmable interconnect structure and provide a self contained integrated circuit architecture which supports basic analog signal processing functions. The analog circuit blocks include basic circuit elements such as operational amplifiers, resistors, and capacitors, which can be programmably connected in a variety of circuit configurations. Users can define the functionality of individual blocks, control their respective characteristics, and interconnect blocks to define an overall architecture. Integrating the elements together in a single integrated circuit has a number of advantages. Critical circuit specifications such as dynamic range and common mode rejection can be more easily controlled, helping to make circuit performance more predictable and reliable. The input and output characteristics of the programmable analog circuit block allow the block to be used within an analog routing pool with other programmable analog circuit blocks to provide more complicated analog circuits without significant degradation in performance. The elimination of external passive components and the addition of programmable interconnect structures for the circuit blocks also reduce the sensitivity of circuit designs to board-level variables and tolerances. Moreover, by removing sensitivity to an analog routing pool and facilitating internal modification of function without changing topologic sensitivity to offset and distortion, an integrated circuit can advantageously be provided with multiple programmable analog circuit blocks and an analog routing pool which can accommodate more complex analog functions.

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L4: Entry 1 of 4 File: USPT Mar 30, 2004

DOCUMENT-IDENTIFIER: US 6714066 B2
TITLE: Integrated programmable continuous time filter with programmable capacitor arrays

Detailed Description Text (3):
Output signals from instrumentation amplifier 120 are sent to 5th order low-pass filter 130. Filter 130 is just one example of a programmable analog block that can be selectively coupled into integrated circuit 100. For example, integrated circuit 100 can include additional programmable analog blocks, for example a high-pass filter that can be programmably selected by a user and thereby coupled into a signal path. For a more general description of programmable analog integrated circuit architectures, see the aforementioned U.S. Pat. No. 5,574,678. Signals then pass from filter 130 to output amplifier 140, and to differential outputs 150.

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L22: Entry 2 of 2 File: USPT Sep 28, 1999

DOCUMENT-IDENTIFIER: US 5960213 A
TITLE: Dynamically reconfigurable multi-function PCI adapter device

Abstract Text (1):
A PCI compliant device having an internal function and a secondary PCI port for a second PCI device having additional functions. The device adapts its internal function and memory and the functions and memory of the second PCI device such that the host system sees only a single multi-function device, which appears to have the combined memories and functions of the adapter and second PCI device. Preferably the adapter itself includes a graphics pre-processor, and is connected to one or more rendering processors on the second PCI port.

Current US Cross Reference Classification (2):
713/1

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